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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,869	06/27/2003	Zhongze Wang	MI22-2343	7086

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,869	ZHONGZE WANG	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-66* is/are pending in the application.

4a) Of the above claim(s) *50-54 and 57-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49,55,56 and 60-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 24, 2005 has been entered.

Claim Objections

Claim 49 is objected to because of the following informalities: In line 27, "silicon-nitride-comprising" should be replaced with –silicon nitride-comprising--. In line 28 "first silicon dioxide layer" should be replaced with –first silicon dioxide-comprising--. Appropriate correction is required.

Claim 62 is objected to because of the following informalities: In line 4, Applicants recite "the insulator layer being formed to comprising:" The examiner believes this contains a typographical error and Applicant intended on reciting –the insulator being formed comprising:--.

In line 9 of claim 62, "silicon nitride-comprising" should be replaced with –silicon nitride comprising--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 49, 62-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. Patent No. 6,661,065) in view of Yu (U.S. Patent No. 6,664,146).

Kunikiyo (see column 26, line 10 through column 28, line 60 and Figure 49) discloses in one embodiment the method of forming silicon-on-insulator comprising integrated circuitry, comprising:

forming a silicon-comprising layer (74) of the silicon-on-insulator circuitry;

forming an insulator layer of the silicon-on-insulator circuitry, the insulator layer being formed to comprise:

a first silicon-dioxide comprising region, in contact with the silicon-comprising layer;

a silicon-nitride-comprising region in contact with the first silicon-dioxide comprising region; and

a second silicon dioxide-comprising region in contact with the silicon nitride-comprising region, the silicon nitride-comprising region being received intermediate the first and second silicon dioxide-comprising regions (see especially column 28, lines 51-55, and column 26, line 5 through column 28, line 55).

forming a pair of source/drain regions (4) in the silicon comprising layer and a channel region (7) in the silicon comprising layer which is received intermediate the source/drain regions, the silicon nitride-comprising region running along at least a portion of the channel region and the first silicon dioxide layer running along at least a portion of the channel region;

forming a transistor gate (90) operably proximate the channel region;

Kunikiyo discloses the method as claimed and rejected above in a first embodiment, but do not disclose the method in which the oxide layers are formed in the ONO stack. Therefore, Kunikiyo does not disclose in the first embodiment the method of forming the insulator layer comprising forming a first silicon dioxide layer on a first substrate, forming a second silicon dioxide layer on a second substrate and joining the first substrate and to the second substrate.

Kunikiyo discloses the method of forming a buried oxide in another embodiment (herein after referred to as the second embodiment) including the forming the insulator layer comprising forming a first silicon dioxide layer on a first substrate, forming a second silicon dioxide layer on a second substrate and joining the first substrate and to the second substrate (see column 26, line 5 through column 27, line 12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of the first embodiment by the method of the second embodiment since as Kunikiyo discloses the method of the second embodiment allows for enhanced reliability of the semiconductor device formed on the SOI substrate (see column 27, lines 1-12), and because as Kunikiyo discloses modifications may be

made to the buried insulating film containing oxide formed by the method of the second embodiment, such as adding a nitride layer to form an ONO stack (see column 28, lines 52-58).

Kunikiyo does not disclose the method wherein the source/drain regions extends to the insulator layer, or wherein the channel region extends less than completely through a thickness of the silicon-comprising layer. Yu disclose the method wherein the source/drain regions extends to the insulator layer, or wherein the channel region extends less than completely through a thickness of the silicon-comprising layer (see Figure 2 and column 2, line 63 through column 3. line 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device such that source/drain regions extends to the insulator layer, and the channel region extends less than completely through a thickness of the silicon-comprising layer, because as Yu teaches that one may form a fully or partially depleted channel region depending on the desired application of the device (see Yu column 2, line 63 through column 3, line 3).

In re claim 62, Kunikiyo (see column 26, line 10 through column 28, line 60 and Figure 49) disclose a method of forming silicon-on-insulator comprising integrated circuitry, comprising:

forming a silicon-comprising layer (74);

forming an insulator layer, the insulator layer being formed comprising:

a first silicon dioxide comprising region in contact with the silicon-comprising layer;

a silicon nitride comprising region in contact with the first silicon dioxide; and

a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride-comprising region being received intermediate the first and second silicon dioxide comprising regions (see especially column 28, lines 51-55, and column 26, line 5 through column 28, line 55);

forming a pair of source/drain regions (4) in the silicon-comprising layer;

forming a channel region (7) in the silicon-comprising layer which is received intermediate the source/drain regions; and

forming a gate structure (90) operably proximate the channel region.

Kunikiyo does not disclose the method wherein the source/drain regions extends to the insulator layer, or wherein the channel region extends less than completely through a thickness of the silicon-comprising layer. Yu disclose the method wherein the source/drain regions extends to the insulator layer, or wherein the channel region extends less than completely through a thickness of the silicon-comprising layer (see Figure 2 and column 2, line 63 through column 3. line 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device such that source/drain regions extends to the insulator layer, and the channel region extends less than completely through a thickness of the silicon-comprising layer, because as Yu teaches that one may form a fully or partially depleted channel region

depending on the desired application of the device (see Yu column 2, line 63 through column 3, line 3).

In re claim 63, Kunikiyo and Yu disclose the method as claimed and rejected above in a first embodiment, but do not disclose the method in which the oxide layers are formed in the ONO stack. Therefore, Kunikiyo does not disclose in the first embodiment the method of forming the insulator layer comprising forming a first silicon dioxide layer on a first substrate, forming a second silicon dioxide layer on a second substrate and joining the first substrate and to the second substrate.

Kunikiyo discloses the method of forming a buried oxide in another embodiment (herein after referred to as the second embodiment) including forming the insulator layer comprising forming a first silicon dioxide layer on a first substrate, forming a second silicon dioxide layer on a second substrate and joining the first substrate and to the second substrate (see column 26, line 5 through column 27, line 12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of the first embodiment by the method of the second embodiment since as Kunikiyo discloses the method of the second embodiment allows for enhanced reliability of the semiconductor device formed on the SOI substrate (see column 27, lines 1-12), and because as Kunikiyo discloses modifications may be made to the buried insulating film containing oxide formed by the method of the second

embodiment, such as adding a nitride layer to form an ONO stack (see column 28, lines 52-58).

Claims 55-56, and 60-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. Patent No. 6,661,065) and Yu (U.S. Patent No. 6,664,146) in view of Xiang (U.S. Patent No. 6,410,938).

In re claims 55-56, Kunikiyo and Yu et al. disclose the method as claimed and rejected above, but does not disclose the method wherein the forming the silicon nitride comprising region comprising nitridizing after forming the joined substrate and wherein the nitridizing comprises ion implanting.

Xiang discloses the method of method wherein the forming the silicon nitride comprising region comprising nitridizing after forming the joined substrate and wherein the nitridizing comprises ion implanting (see column 2, lines 40-50, column 3, lines 30-41 and column 4,lines 34-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have nitridized after joining the substrates and the nitridizing comprises ion implanted rather than the deposition method of Kunikiyo because as Xiang discloses the nitridizing method allows for a high quality nitride that reduces or prevents depletion of dopant material from the channel regions (see column 1, lines 40-55).

In re claim, 60, the combined method of Kunikiyo and Xiang teach that the silicon nitride comprising region is formed to have a thickness of from about 10 Angstroms to about 50 Angstroms (see Xiang column 3, lines 30-40).

In re claim 61, neither Kunikiyo nor Xiang teach the method wherein the first silicon dioxide comprising region is formed to have a thickness of from about 10 Angstroms to about 50 Angstroms.

The examiner notes that Applicant does not teach that the thickness range solves any stated problem or is for any particular purpose. Therefore, the thickness range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon oxide to a thickness of form about 10 Angstroms to about 50 Angstroms, since the invention would perform equally well when the insulating layer of the SOI substrate is formed to a different thickness and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 64-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. Patent No. 6,661,065) and Yu (U.S. Patent No. 6,664,146) in view of Henley et al. (U.S. Patent No. 6,048,411).

Kunikiyo and Yu disclose the method as claimed and rejected above, but do not disclose the method wherein the joining comprises applying a voltage to the first substrate and the second substrate and wherein after joining the first and second substrates, thinning the joined substrate, and wherein thinning comprises removal of a portion of the silicon-comprising layer.

Henley et al. disclose the method wherein the joining comprises applying a voltage to the first substrate and the second substrate and wherein after joining the first and second substrates, thinning the joined substrate, and wherein thinning comprises removal of a portion of the silicon-comprising layer (see column 8, lines 31-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a voltage to the substrate to create the bond because as Henley et al. teach the method reduces the amount of crystal defects introduced and reduces damage (see column 8, lines 31-45). Further it would have been obvious to one of ordinary skill in the art at the time the invention was made to thin the substrate by removal of a portion of the silicon-comprising layer in order to form a smooth and planar surface for device formation.

Response to Arguments

Applicant's arguments with respect to claims 49 and 55-56 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk